Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 15. This sheet replaces the original sheet that included FIG. 15. In FIG. 15, "(PRIOR ART)" has been added.

Remarks

Claims 1, 2, 5, 7-9, and 19-25 are pending in the application, of which claims 1 and 2 are in independent form. Claims 1, 2, 9, 19 and 20 have been amended. Claims 26-32 have been added. Claims 3, 4, 6 and 15-18 have been canceled.

The Examiner has requested that FIG. 15 be designated as "prior art." In response, applicants have enclosed a replacement sheet that indicates that FIG. 15 is prior art.

The Examiner has rejected claims 9 and 18-20 under 35 USC 112, second paragraph, for being indefinite. Applicants have included amendments to clarify that the first angle is formed by a first imaginary line connecting the middle of the first junction face width with the middle of the second junction face width and a second imaginary line extending in the direction of the grain boundary and the second angle is defined by respective imaginary lines connecting first ends of the first junction face width and second ends of the second junction face width. Applicants note that while the junction faces may be parallel, their face widths differ (claim 2) so that connecting the ends of the face widths form lines that are not parallel. Applicants request, therefore, that this rejection be withdrawn.

The Examiner has rejected claims 2 and 3 under 35 USC 102(b) for anticipation by Neider et al. (U.S. Pat. No. 5,385,865); claim 1 under 35 USC 103(a) for obviousness over Neider et al.; and claims 4-9, 15-19, and 20-25 under 35 USC 103(a) for obviousness over Neider et al. in combination with Taketomi et al. (U.S. Pat. Pub. No. 2003/0022471A1). Applicants respond as follows.

Neider et al. provide no description of a thin film transistor. Their two gate electrodes provided on an active layer are insulated by mesa etched trenches provided in the active layer. The planar shape of their active layer is rectangular forming two gate transistors such that an electric field from the two gate electrodes acts so as to control movement of an electron. Their semiconductor layer is an epitaxial growth layer. They do not disclose grain in the active layer, nor suggest grain and mobility of a hole and an electron.

Taketomi et al. describe a thin film transistor and seek high field effect mobility. Their semiconductor film is a polycrystalline silicon film in which crystal nuclei generated in the periphery by irradiation of an amorphous silicon with a laser beam grows into the center. See Paragraph [0110] (from line 6). "Specifically, crystallization is effected while .... can be formed."

In some of applicants' embodiments, the planar shape of the active layer is trapezoidal. The active layer may have no mesa etched trenches. The gate electrode can be configured to cover the whole area between the source and drain regions with one gate electrode. Regarding the semiconductor layer, the amorphous semiconductor film can be a crystallized film irradiated with a laser beam which is weak at the center and strong in the periphery.

Applicants have amended claim 1 to specify that the semiconductor device is a thin film device. Claim 2 has been amended to include the trapezoidal shape and opening angle limitations of previous claims 3 and 4, which have been canceled. Claims 6 and 15-18, which depended directly or indirectly from claims 3 and 4 have been canceled. The inventions claimed in claims 1 and 2 are not suggested by Neider et al. or Taketomi et al., either singly or in combination, and are not mere optimizations through routine experimentation. Applicants request, therefore, that these rejections be withdrawn.

Claims 26-32 are new and depend from what applicants believe to be allowable claims and should, therefore, be allowed as well.

Applicants believe the application is in condition for allowance and respectfully requests the same.

Respectfully submitted,

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